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Solid state image pick-up device e.g. CCD - uses timing generator to generate higher frequency clock signal than in normal operation during power on or release power save mode

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Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 7030819	A	19950131	JP 93194315	A	19930708	199514 B
US 5777671	A	19980707	US 94268571	A	19940706	199834
			US 96586304	A	19960117	

Priority Applications (No Type Date): JP 93194315 A 19930708

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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JP 7030819	A		6	H04N-005/335	
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US 5777671	A			H04N-003/14	Cont of application US 94268571
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Abstract (Basic): JP 7030819 A

The image pick-up device consists of a sequence of sensors (11) which output an image signal. On detection of this image signal, a charge detector (14) converts this image signal into its equivalent electrical signal. At the time of switch ON of power supply source or release to a power save mode, the control signal (Vc) generated in a control circuit (17) rises from the low level to high level in the transition time.

The clock signal (phi1) of the timing generator (16) is generated. The clock signal is higher than the clock signal (phi2) generated during the normal operation. The first clock signal is input to the CCD shift register (13).

ADVANTAGE - Provides high speed transmission of invalid charge. Reduces transition time of solid state image pick-up device coming to state of normal operation. Obtains low power consumption.